NEW DATA UPDATE 2

NATIONAL SEMICONDUCTOR

JANUARY 1981

NEW DATA UPDATE 2

NATIONAL SEMICONDUCTOR

The New Data Update 2 is a service of National Semiconductor to keep you abreast of the latest products available. This issue features the first pages of data sheets published October through December 1980 (1 quarter). Subsequent issues will be published quarterly. An alpha-numerical index by device number, an index by device function, a listing of new application notes and briefs are included in the front section.

Circle the appropriate update number on the business reply card (centerfold) and drop in the mailbox to receive the complete data sheet or publication of your choice. For any publication without an update number, please fill in application note number or brief number in blank spaces provided on reply card.

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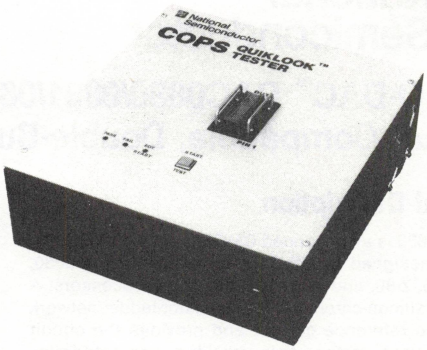
National Semiconductor

October 1980



COPS QUIKLOOK™ TESTER: COP400-TO1

Supports the Entire COP400 Microcontroller Family

- **Hardware:**

  Tester Chassis, Component Interface Cards (4), Diagnostic Card, Development System/Quiklook Cables (2)

- **Software:**

  Master diskette contains programs for use with COP400-PDS Development System

Easy to Use Features

- Tester Diagnostics
- Automatic Chip Handler Interface
- Test Generation Program

Product Overview

The COPS QUIKLOOK TESTER provides a simple but effective means to perform incoming inspection of the National Semiconductor Corporation COP400 family. The QUIKLOOK TESTER, under the control of the COP400-PDS Development System, provides GO, NO-GO functional tests for COP400 devices.

Comprehensive Test Capability

The following COP400 features are tested at 5 Volts

a) Maximum frequency operation
b) Chip I/O functionality
c) Register/memory reference instructions
d) Arithmetic instructions
e) Branch instructions
f) ROM
g) RAM
h) CKO xtal output (optional)
i) Interrupts (optional)
j) Multicop sync (optional)
k) Low power reset (optional 444L/445L only) (4.3 volts)
l) Dual clock (optional 420C/421C only)
m) CKO as a general purpose input (optional)
n) RAM keep alive (optional)
o) MICROBUS™ (optional)

Diagnostics

Tests QUIKLOOK system hardware for correct operation

Test Generation Program

The test generation program is used to generate test patterns for comparison with incoming masked parts. The resulting patterns are stored on the development system diskette for loading into the QUIKLOOK TESTER at run time.

Order Information

COP400-TO1 (60 Hz 120 V_{AC})
COP400-TO1E (50 Hz 220 V_{AC})

Documentation

420306199-001 Operators Manual

Software

440306199-200 Master Diskette

Note: To be used with COPS Development System

COP400-PDS (60 Hz 120 V_{AC})
COP400-PDSE (50 Hz 220 V_{AC})

Environmental Requirements

Operating and Storage Temperature 50° to 125°F
Relative Humidity 8% to 80%
Maximum Wet Bulb Temperature 85°F

Shipping
Temperature −40° to 125°F
Relative Humidity 8% to 80%
Maximum Wet Bulb Temperature 85°F

Power
115 Volts AC ±10%, 60 Hz, 24 watts
230 volts AC ±10%, 50 Hz, 27.69 watts

Physical Specifications
Height 5¾″, Width 14″, Depth 15½″

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National Semiconductor

DECEMBER 1980

MICRO-DAC™ DAC0830/0831/0832
8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z-80, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC's™). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

Micro-Dac is a trademark of National Semiconductor Corp.

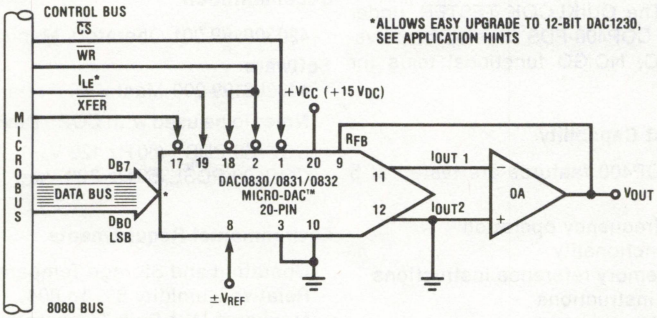
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired

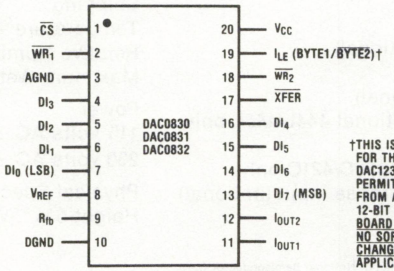
Key Specifications

Current settling time	1 μs
Resolution	8-bits
Linearity (guaranteed over temp.)	8, 9, or 10 bits
Gain Tempco	0.0002% FS/°C
Low power dissipation	20 mW
Single power supply	5 to 15 V_{DC}

Typical Application



Pin Configuration Top View



†THIS IS NECESSARY FOR THE 12-BIT DAC1230 SERIES TO PERMIT INTERCHANGING FROM AN 8-BIT TO A 12-BIT DAC WITH NO PC BOARD CHANGES AND NO SOFTWARE CHANGES. SEE APPLICATIONS SECTION.

Circle DATA UPDATE No. 1107

National Semiconductor

OCTOBER 1980

MICRO-DAC:™ DAC1000/1/2 and DAC1006/7/8, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1000/1/2 and DAC1006/7/8 are advanced CMOS/Si-Cr 10-, 9- and 8-bit accurate multiplying DACs which are designed to interface directly with the 8080, 8048, 8085, Z-80 and other popular microprocessors. These DACs appear as a memory location or an I/O port to the μP and no interfacing logic is needed.

These devices, combined with an external amplifier and voltage reference, can be used as standard D/A converters; and they are very attractive for multiplying applications (such as digitally controlled gain blocks) since their linearity error is essentially independant of the voltage reference. They become equally attractive in audio signal processing equipment as audio gain controls or as programmable attenuators which marry high quality audio signal processing to digitally based systems under microprocessor control.

All of these DACs are double buffered. They can load all 10 bits or two 8-bit bytes and the data format can be either right justified or left justified. The analog section of these DACs is essentially the same as that of the DAC1020.

The DAC1000 series are the 10-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC's™). For applications requiring other resolutions, the DAC0830 series (8 bits) and the DAC1208 and DAC1230 (12 bits) are available alternatives.

Part #	Accuracy (bits)	Pin	Description
DAC1000	10	24	Has all logic features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For left-justified data
DAC1007	9		
DAC1008	8		

MICRO-DAC™ is a trademark of National Semiconductor Corp.

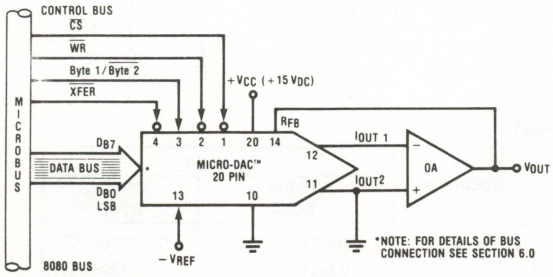
Features

- Uses easy to adjust END POINT specs, NOT BEST STRAIGHT LINE FIT
- Low power consumption
- Direct interface to all popular microprocessors.
- Integrated thin film on CMOS structure
- Double-buffered, single-buffered or flow through digital data inputs.
- Loads two 8-bit bytes or a single 10-bit word.
- Logic inputs which meet T^2L voltage level specs (1.4 V logic threshold).
- Works with ±10V reference — full 4-quadrant multiplication.
- Operates STAND ALONE (without μP) if desired.
- Available in 0.3″ standard 20-pin and 0.6″ 24-pin package.
- Differential non-linearity selection available as special order.

Key Specifications

- Output Current Settling Time — 500 ns
- Resolution — 10 bits
- Linearity — 10, 9, and 8 bits (guaranteed over temp.)
- Gain Tempco — −0.0003% of FS/°C
- Low Power Dissipation (including ladder) — 20 mW
- Single Power Supply — 5 to 15 V_{DC}

Typical Application



DAC1006/1007/1008

Circle DATA UPDATE No. 1108

December 1980

National Semiconductor

MICRO-DAC™ DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232 12-Bit, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

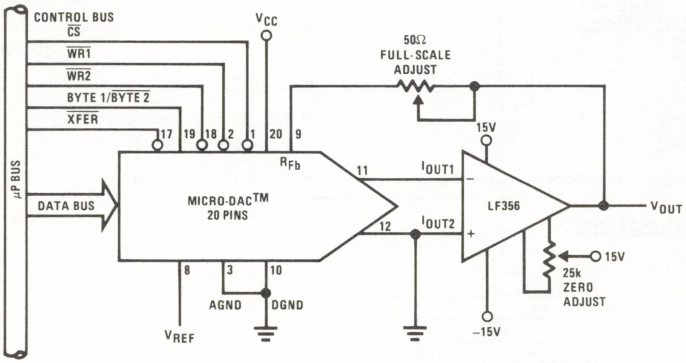
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

Current Settling Time	1 μs
Resolution	12 Bits
Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
Gain Tempco	1.5 ppm/°C
Low Power Dissipation	20 mW
Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



Ordering Information

Accuracy	Package	
	20-Pin D20A	24-Pin D24C
0.012%	DAC1230LCD	DAC1208LCD
0.024%	DAC1231LCD	DAC1209LCD
0.05%	DAC1232LCD	DAC1210LCD

MICRO-DAC™ is a trademark of National Semiconductor Corp.

National Semiconductor

December 1980

DAC1218, DAC1219 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved through the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors to allow the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

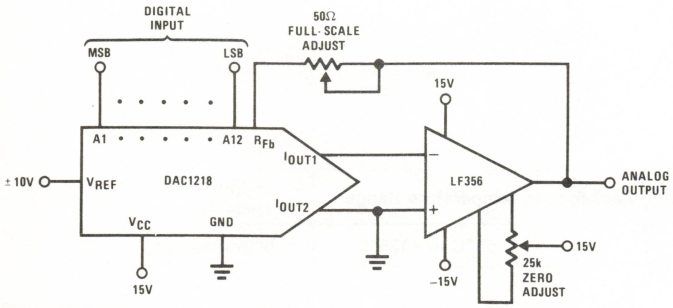
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

Current Settling Time	1 μs
Resolution	12 Bits
Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
Gain Tempco	1.5 ppm/°C
Low Power Dissipation	20 mW
Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application

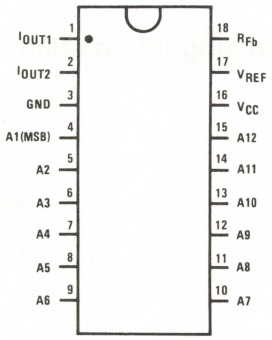


$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



TOP VIEW

National Semiconductor

OCTOBER 1980

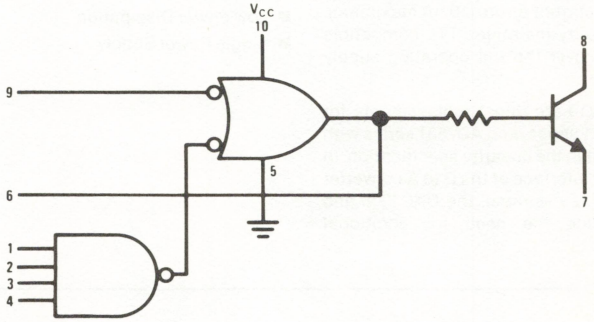
DH0011A High Voltage High Current Driver

General Description

The DH0011A High Voltage, High Current Driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 50V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

Logic Diagram



Ordering Information

NSC Designation	Package	Temperature Range	Output Capability
DH0011AH	H10C	−55°C to +125°C	500 mA

National Semiconductor

OCTOBER 1980

DP8350 Series CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits. Three standard products are available, designated DP8350, DP8352, DP8353. Custom devices, however, are available in a broad range of mask programmable options.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock may be inputted to the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMs, or DM86S64-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, vertical blanking, horizontal sync, and vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame
- Format of Video Outputs

The CRTC also provides system sync and program inputs including Refresh Control, Reset, and Address Mode.

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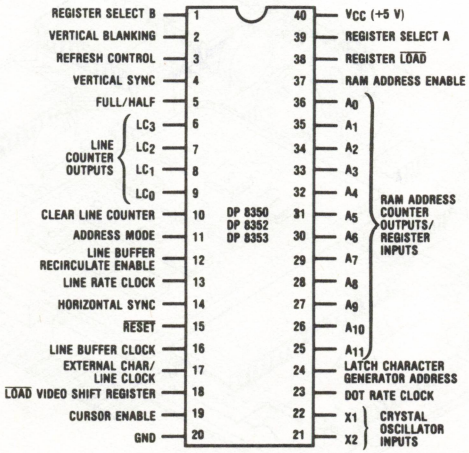
Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Internal top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 2 programmable refresh rates, pin selectable
- Programmable characters/row (128 max.)
- Progammable character field size (up to 16 dots × 16 scan line field size)
- Programmable scan lines/frame (512 max.)
- Programmable character rows/frame
- Single +5V power supply
- Inputs and outputs TTL compatible
- Direct interface with DM86S64 character generator
- Ease of system design/application

Connection Diagram



Ordering Information:

DP8350N
DP8352N
DP8353N

National Semiconductor

December 1980

DT1000 DIGITALKER™ Speech Synthesis Evaluation Board

General Description

The DIGITALKER™ (DT1000) speech synthesis evaluation board is an extremely easy to use device for understanding the operation and application of the DIGITALKER chip set in an end product.

The DT1000 contains all components required to output speech upon demand: a speech processor chip (SPC), 2 MAXI-ROMs® containing 138 individual words, linear filter, audio amplifier, keyboard, and a COPS™ microcontroller complete with stored data programmed to provide the various functions on the board. The only external hardware required for complete operation are a single 7V–11V power supply, a speaker of your choice for size and quality, and this instruction sheet.

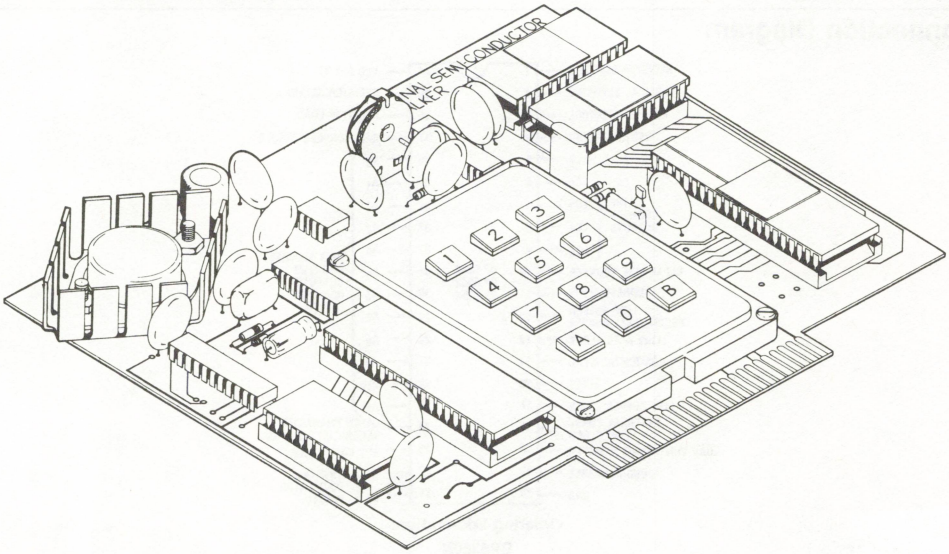
The 2 speech MAXI-ROMs employed on the board contain a brief introductory phrase, 138 separate and individual words consisting of numbers and letters of the alphabet, assorted useful nouns, verbs and tones; and 5 different individual silence durations. (In constructing a phrase, different silence durations between different words significantly affect the overall quality of the phrase.)

A COPS program is provided which permits the user to: 1) sequentially output each word automatically; 2) repeat any desired word; 3) build and store several short phrases for outputting when desired; 4) output a "canned" phrase which permits insertions and changing of a word in the phrase; 5) play a simple game which requires some interaction between the keyboard and the user; and 6) output hex equivalent decimal number inputs.

Features

- Only a single 7V–11V power supply and inexpensive loudspeaker required for total operation
- 138 individually addressable words, applicable to many products
- Programmed COPS processor permits 6 individual program modes
- Demonstrates the extreme flexibility and ease of application of the DIGITALKER chip set
- 1/2 watt audio amplifier on-board
- Edge connector facilitates tying in to external processor system (3M Company connector part number #3415)

DT1000 Conceptual Drawing



MAXI-ROM® is a registered trademark of National Semiconductor Corp.
DIGITALKER™ and COPS™ are trademarks of National Semiconductor Corp.

Circle DATA UPDATE No. 1113

National Semiconductor

December 1980

DT1050 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1050 is a standard DIGITALKER kit encoded with 137 separate and useful words, 2 tones, and 5 different silence durations. (See the Master Word List Table I). The words and tones have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1050 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

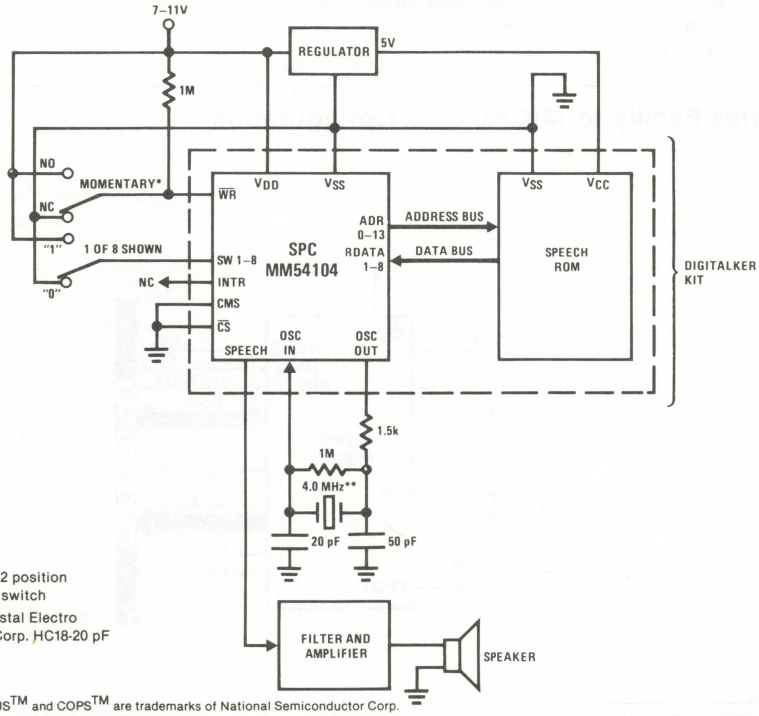
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- 144 addressable expressions, including numbers
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

DIGITALKER™, MICROBUS™ and COPS™ are trademarks of National Semiconductor Corp.

National Semiconductor

October 1980

INS8070-Series Microprocessor Family

General Description

The INS8070-Series of microprocessors (hereinafter referred to as the 70-Series Family) is intended for use in systems requiring the economy of a single chip, the flexibility of multiprocessing bus architecture and the power of 16-bit arithmetic operations.

Designed for simplicity and low-cost implementation for stand-alone multiprocessing and DMA systems, the members of the 70-Series family include:

INS8070 - 64 Bytes of RAM, no ROM
INS8072 - 64 Bytes of RAM, 2.5K ROM

The 70-Series family comprises bus-oriented microprocessors with on-board ROM and RAM and built-in multi-processing logic. Low-cost systems containing data may occupy the same bus and still run at full speed, as their external bus requirements are confined to the occasional access of data. Such systems include terminals, intelligent peripherals and multiprocessing systems (e. g., the solution of polynomials in real-time).

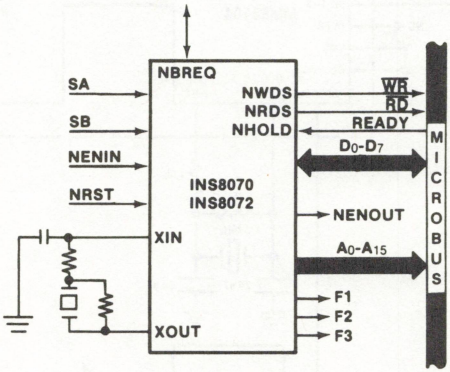
For very high-volume users, the instruction set, ROM and RAM size may be tailored to fit the necessary applications.

The 70-Series family is fabricated using National's Standard N-channel, silicon gate, depletion load, MOS technology. All the devices are housed in standard 40-pin dual-in-line packages.

Features

- On-Board ROM
- On-Board RAM (Executable)
- 8-Bit Data Bus
- 16-Bit Address Bus (64K Addressing Capability)
- Comprehensive Set of 8 and 16-Bit Arithmetic, Logic and Stack Manipulation Instructions
- Hardware 16 x 16 Bit Multiply (37 μs) and Divide (42 μs)
- Built-in Multiprocessing and DMA Logic
- Interfaces with Memory and Standard INS8080 Peripherals at Any Clock Speed
- On-Chip Clock Generation
- Single Instruction Character Search and Single Instruction ASCII to Decimal Conversion
- Full Hardware and Software Development Systems Available on STARPLEX ™ and ISE ™
- Single 5-Volt Supply
- MICROBUS™ Compatible

70-Series Family to MICROBUS Configuration



Circle DATA UPDATE No. 1115

National Semiconductor

November 1980

INS8251 Programmable Communication Interface

General Description

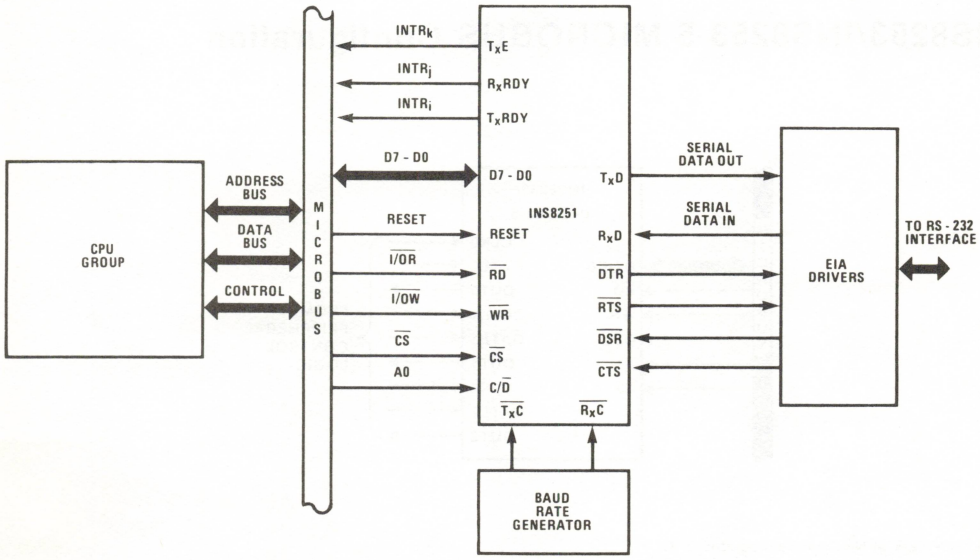
The INS8251 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in National Semiconductor's N8080 microcomputer family. The functional configuration of the INS8251 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communication signal presently in use (including IBM Bisync).

The INS8251 can be programmed to receive and transmit either synchronous or asynchronous serial data. The INS8251 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8251 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the INS8251, as well as any transmission error conditions (parity, overrun, or framing).

Features

- Synchronous and Asynchronous Full Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Internal or External Character Synchronization
  - Automatic Sync Insertion
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - 3 Selectable Clock Rates (1x, 16x or 64x the Baud Rate)
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
- Baud Rates
  - DC to 56k Baud (Synchronous Mode)
  - DC to 9.6k Baud (Asynchronous Mode)
- Transmission Error Detection Capabilities
  - Parity
  - Overrun
  - Framing
- Double Buffering of Data
- TTL Compatible
- Single TTL Clock
- Reduces System Component Count
- MICROBUS™* Compatible

INS8251 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Circle DATA UPDATE No. 1116

National Semiconductor

November 1980

INS8253/INS8253-5 Programmable Interval Timer

General Description

The INS8253 is a programmable timer/counter device contained in a standard, 24-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, provides counting or time-out services in a microcomputer system. The various operating modes and other functional characteristics of the INS8253 are programmed by the system software.

The INS8253 provides three independent 16-bit down counters, each of which is capable of count rates in the range DC to 2MHz. Through software initialization, each counter can be made to operate in any one of six modes. The modulus and counting system used are also specified by system software. The operating characteristics of any individual counter can be modified by the software at any time to meet changing system requirements.

The modulus of any given counter can be changed at the program's discretion by loading a new value into the counter. A counter load operation may be limited to the counter's least significant byte or to its most significant byte, or it may revise both halves of the counter.

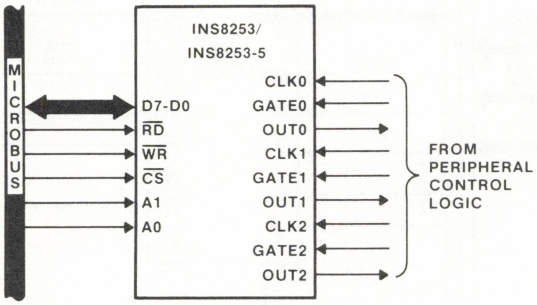
Count sequences may be in either binary or BCD. This choice is also individually specified for each counter by the software.

The contents of each counter may be read either directly or through an auxiliary register. A direct reading of the counter can be made whenever the counter is inhibited from counting. A count value can also be read without interfering with the counting process. This is done by transferring the counter's current value to an auxiliary register and then reading that register. This counter-to-register transfer can be executed without affecting the normal count sequence.

Features

- 3 Individually Programmable 16-Bit Counters
- 6 Operating Modes
- DC to 2MHz Count Rates
- Individual Count Rate and Modulus for Each Counter
- Selectable Counting System (Binary or BCD) for Each Counter
- TRI-STATE® TTL Drive Capability for Bidirectional Data Bus
- Single +5 Volt Power Supply
- 24-Pin Dual-in-Line Package
- MICROBUS™* Compatible
- INS8253-5 for High-Speed Applications

INS8253/INS8253-5 MICROBUS Configuration



*A trademark of National Semiconductor Corp.

Circle DATA UPDATE No. 1117

National Semiconductor

November 1980

INS8255 Programmable Peripheral Interface

General Description

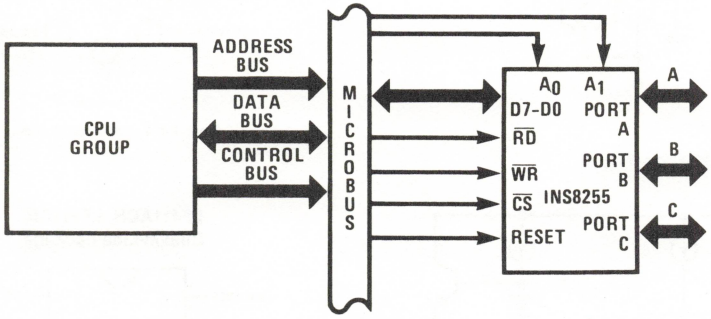
The INS8255 is a programmable peripheral interface contained in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a general-purpose parallel input/output interface in National Semiconductor's 8080 microcomputer family. The functional configuration of the INS8255 is programmed by the system software so that normally no external logic is required to interface peripheral devices.

The INS8255 has three basic modes of operation that can be selected by the system software. In the first mode (Mode 0), the INS8255 provides simple input and output operations for three 8-bit ports. Data is simply written to or read from a specified port (Port A, B or C) without the use of "handshaking" signals. In the second mode (Mode 1), the INS8255 enables the transfer of input/output data to or from a specified 8-bit port (Port A or B) in conjunction with strobes or "handshaking" signals. Ports A and B use the lines of Port C in this mode to generate or accept the "handshaking" signals with the peripheral device. In the third mode (Mode 2), the INS8255 enables communications with a peripheral device or structure via one bidirectional 8-bit bus port (Port A). "Handshaking" signals are provided over the lines of Port C in this mode to maintain proper bus flow discipline.

Features

- Outputs Source 1 mA at 1.5 Volts
- 24 Programmable Input/Output Pins
- Direct Bit Set/Reset Capability
- TTL Compatible
- Reduces System Component Count
- MICROBUS™* Compatible

INS8255 MICROBUS Configuration

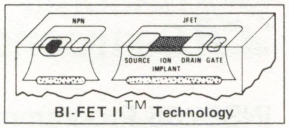


Typical Diagram of MODE 0 operation. The 8 bit ports A, B, C are defined by the user's program to be either an input or an output from/to the peripherals.

*Trademark, National Semiconductor Corp.

National Semiconductor

December 1980



LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

PRELIMINARY

General Description

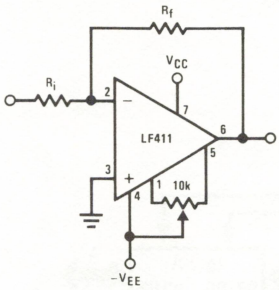
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

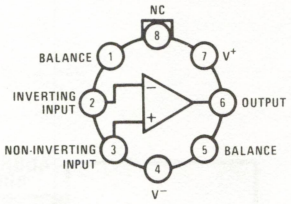
■ Internally trimmed offset voltage	0.5 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	< 0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



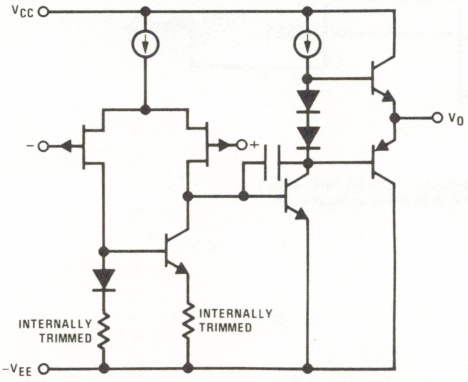
Connection Diagrams

LF411AMH/LF411MH, LF411ACH/LF411CH
Metal Can Package

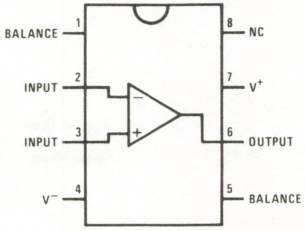


Note. Pin 4 connected to case.

Simplified Schematic



LF411ACN, LF411CN
Dual-In-Line Package

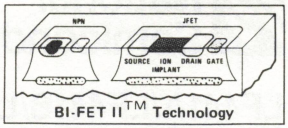


BI-FET II™ is a trademark of National Semiconductor Corp.

Circle DATA UPDATE No. 1119

National Semiconductor

December 1980



LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

PRELIMINARY

General Description

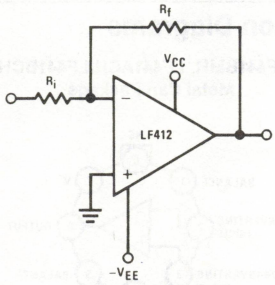
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

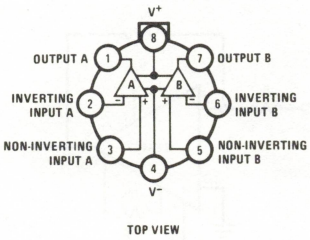
- Internally trimmed offset voltage — 1 mV (max)
- Input offset voltage drift — 10 μV/°C (max)
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth — 3 MHz (min)
- High slew rate — 10V/μs (min)
- Low supply current — 1.8 mA/Amplifier
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection



Connection Diagrams

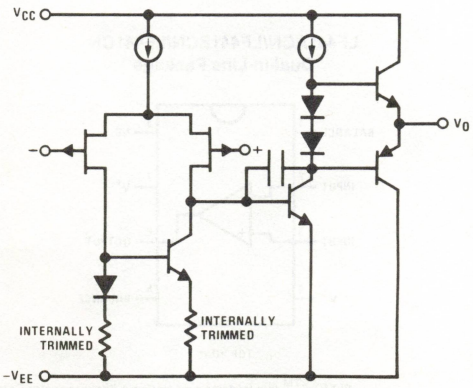
LF412AMH/LF412MH, LF412ACH/LF412CH
Metal Can Package



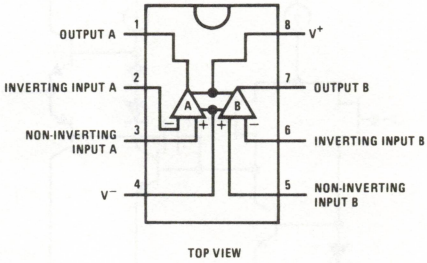
Note. Pin 4 connected to case.

Simplified Schematic

1/2 Dual



LF412ACN, LF412CN
Dual-In-Line Package



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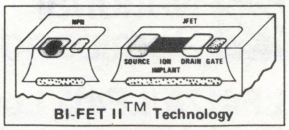
National Semiconductor

December 1980



LF441A/LF441B/LF441 Low Power JFET Input Operational Amplifier

PRELIMINARY

General Description

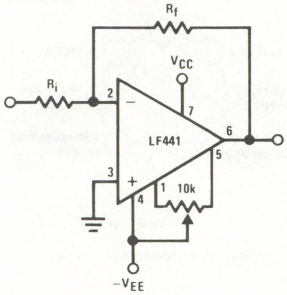
The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441 is pin compatible with the LM741 allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used anywhere low power dissipation and good electrical characteristics are the major considerations.

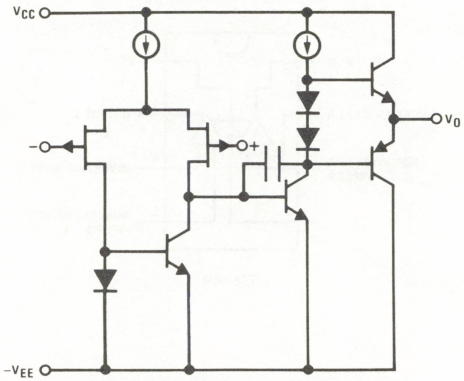
Features

■ 1/10 supply current of a LM741	200 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	0.5 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	40 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	10^{12}Ω
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection

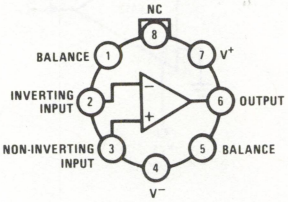


Simplified Schematic



Connection Diagrams

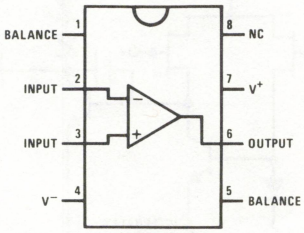
LF441AMH/LF441BMH, LF441ACH/LF441BCH/LF441CH
Metal Can Package



TOP VIEW

Note. Pin 4 connected to case.

LF441ACN/LF441BCN/LF441CN
Dual-In-Line Package



TOP VIEW

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1121 1122 1123 1124 1125 1126 1127 1128 1129 1130 1131 1132 1133 1134 1135
1136 1137 1138 1139 1140 1141 1142 1143 ___ ___ ___ ___ ___ ___ ___
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City _____ State _____ Zip _____

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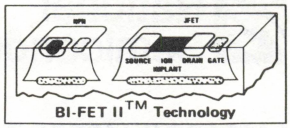
National Semiconductor

December 1980



LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

PRELIMINARY

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

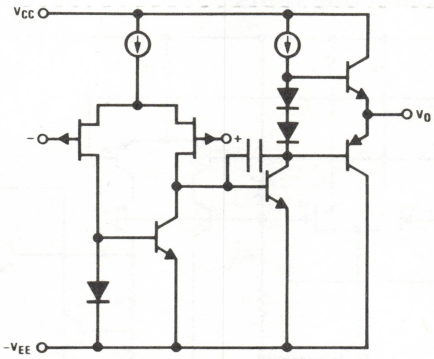
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/4 supply current of a LM148	200 μA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	40 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	10^{12} Ω
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

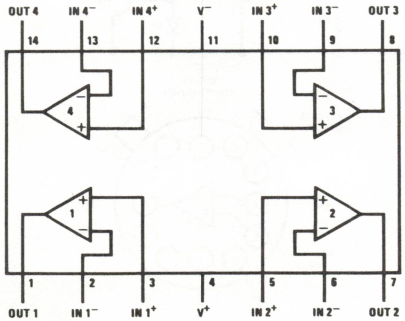
Simplified Schematic

1/4 Quad



Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN
Dual-In-Line Package



TOP VIEW

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Circle DATA UPDATE No. 1122

National Semiconductor

DECEMBER 1980

LH0032/LH0032C Ultra Fast FET Operational Amplifier

General Description

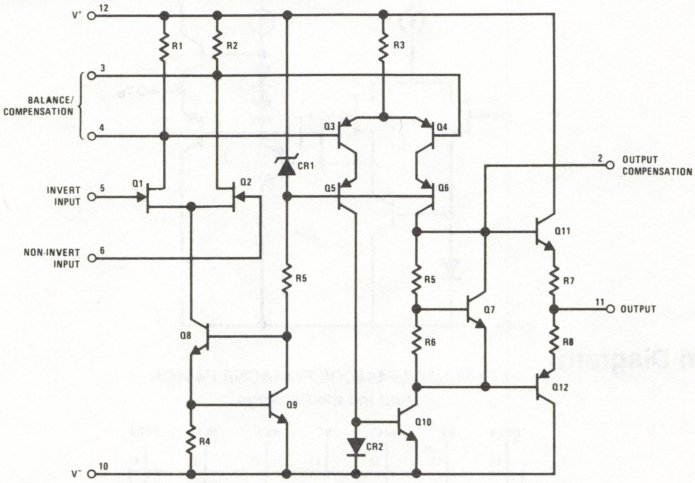
The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

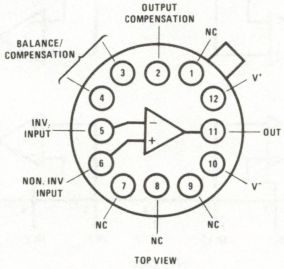
Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range −55°C to +125°C and the LH0032C is guaranteed from −25°C to +85°C.

Schematic and Connection Diagrams





Circle DATA UPDATE No. 1123

National Semiconductor

November 1980

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

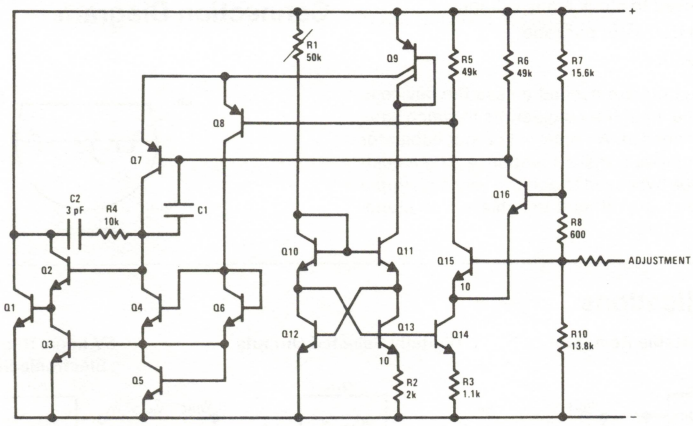
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

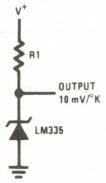
- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

Schematic Diagram

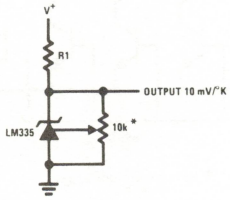


Typical Applications

Basic Temperature Sensor

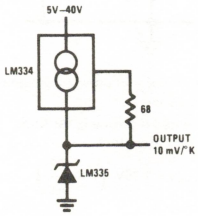


Calibrated Sensor



* Calibrate for 2.982V at 25°C

Wide Operating Supply



Circle DATA UPDATE No. 1124

National Semiconductor

December 1980
PRELIMINARY

LM317L 3-Terminal Adjustable Regulator

General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM317L is packaged in a standard TO-92 transistor package. The LM317L is rated for power dissipations of 625 mW over a 0°C to +125°C range.

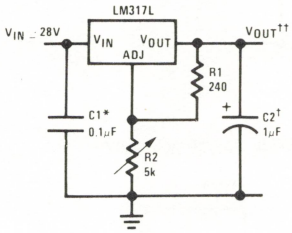
For applications requiring greater output current in excess of 3A and 5A, see LM150 series and LM138 series data sheets, respectively. For the negative complement, see LM137 series data sheet.

Connection Diagram

BOTTOM VIEW

Typical Applications

1.2V–25V Adjustable Regulator

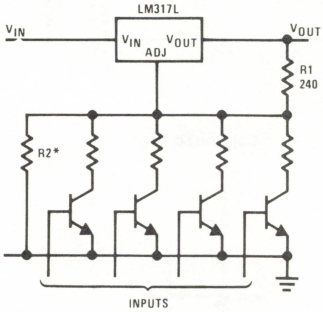


† Optional—improves transient response

* Needed if device is far from filter capacitors

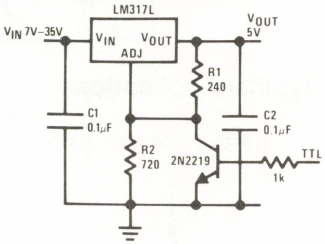
$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

Digitally Selected Outputs



* Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



* Minimum output ≈ 1.2V

National Semiconductor

October 1980

LM1868 AM/FM Radio System

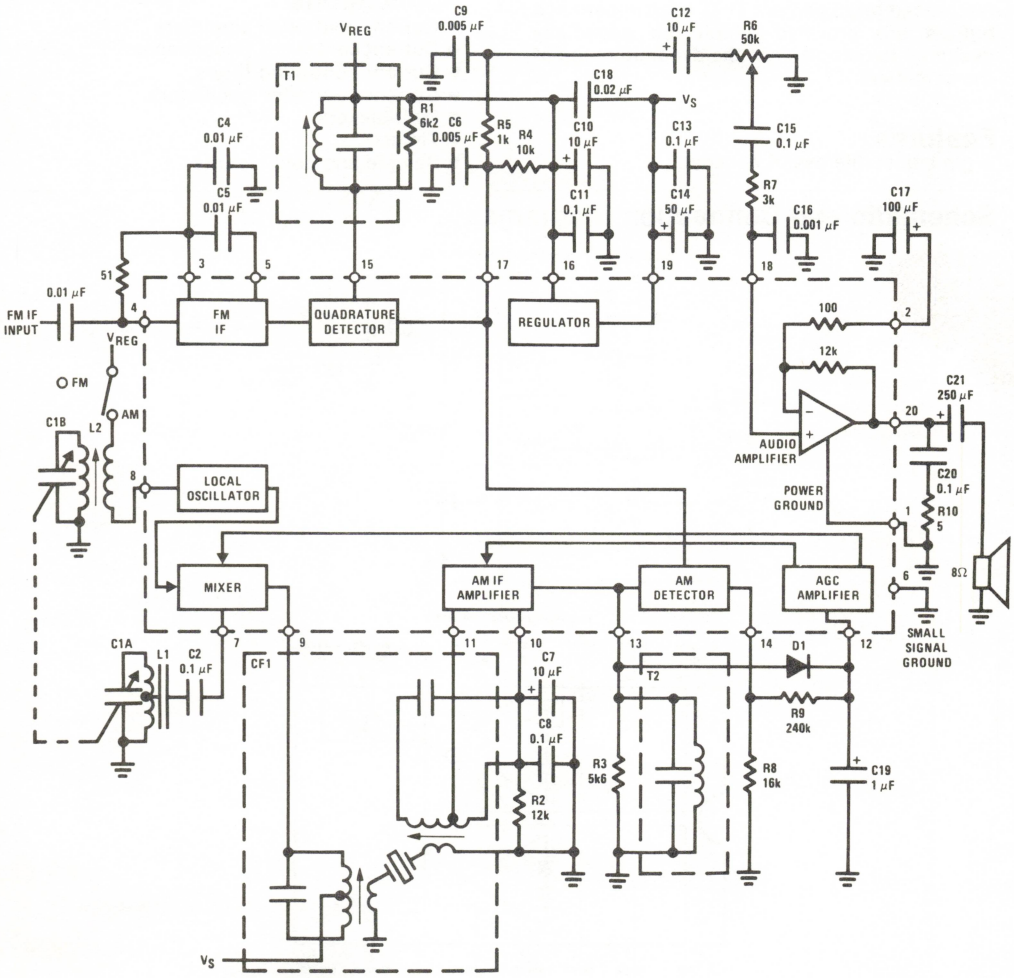
General Description

The combination of the LM1868 and an FM tuner will provide all the necessary functions for a 0.5 watt AM/FM radio. Included in the LM1868 are the audio power amplifier, FM IF and detector, and the AM converter, IF, and detector. The device is suitable for both line operated and 9V battery applications.

Features

- DC selection of AM/FM mode
- Regulated supply
- Audio amplifier bandwidth decreased in AM mode, reducing amplifier noise in the AM band
- AM converter AGC for excellent overload characteristics
- Low current internal AM detector for low tweet radiation

Block Diagram



Note: See table for coil data

Circle DATA UPDATE No. 1126

National Semiconductor

October 1980

LM13700/LM13700A/LM11700A Dual Operational Transconductance Amplifiers With Linearizing Diodes and Buffers

General Description

The LM13700 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The results is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

Features

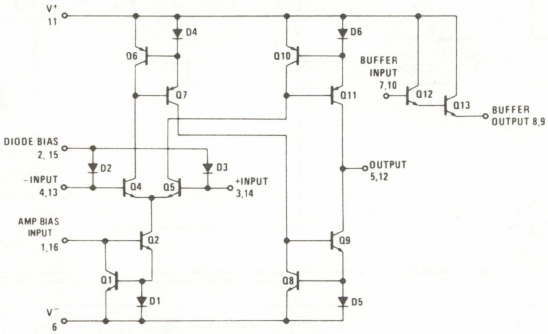
- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal to noise ratio
- Wide supply range ± 2V to ± 22V.

Applications

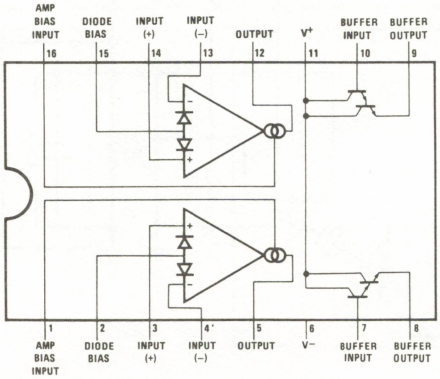
- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Schematic and Connection Diagrams

ONE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



DUAL IN-LINE PACKAGE TOP VIEW



Circle DATA UPDATE No. 1127

National Semiconductor

December 1980

MM54104 DIGITALKER™ Speech Synthesis System

General Description

The DIGITALKER is a speech synthesis system consisting of multiple N-channel MOS integrated circuits. It contains an MM54104 speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed. This can be expanded with minimal external logic.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

Encoding (digitizing) of custom word or phrase lists must be done by National Semiconductor. Customers submit to the factory high quality recorded magnetic reel to reel tapes containing the words or phrases to be encoded. National Semiconductor will sell kits consisting of the SPC and ROM(s) containing the digitized word or phrases.

Features

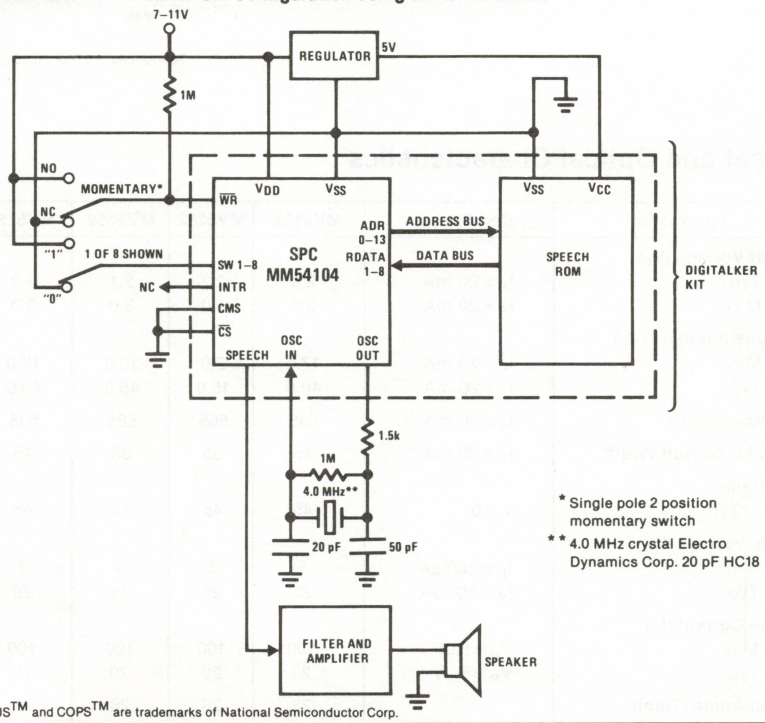
- Designed to be easily interfaced to most popular microprocessors
- 256 possible addressable expressions
- Male, female, and children's voices
- Any language
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- MICROBUS™ and COPS™ compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Easily expandable to greater than 128k ROM
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Ability to store silence durations for timing sequences

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. 20 pF HC18

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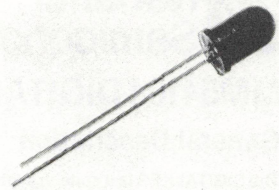
Circle DATA UPDATE No. 1128

National Semiconductor

October 1980



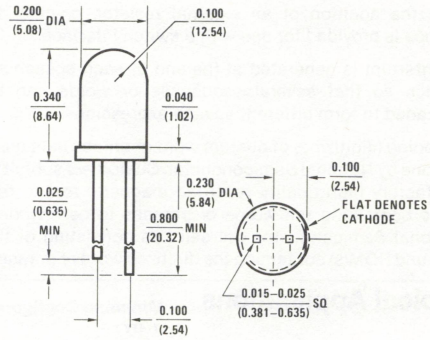
MV5X52 Series LED Lamps

MV5152 Orange Emitter, Transparent Orange Lens
MV5252 Green Emitter, Transparent Green Lens
MV5352 Yellow Emitter, Transparent Yellow Lens
MV5752 Orange-Red Emitter, Transparent Red Lens

Product Description

The MV5X52 LED lamp series are LED emitters packaged in a plastic non-diffused lens of the same color as light from emitter.

Physical Dimensions inches (millimeters)



Tolerances ±0.010(±0.254)

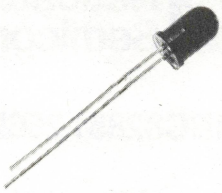
Electrical and Optical Characteristics

Parameter	Conditions	MV5152	MV5252	MV5352	MV5752	Units
Forward Voltage (V_F)						
Typ	$I_F = 20$ mA	2.0	2.2	2.1	2.0	V
Max	$I_F = 20$ mA	3.0	3.0	3.0	3.0	V
Luminous Intensity (V_L)						
Min	$I_F = 20$ mA	17.0	2.0	10.0	17.0	mcd
Typ	$I_F = 20$ mA	40.0	15.0	45.0	40.0	mcd
Peak Wavelength	$I_F = 20$ mA	635	565	585	635	nm
Spectral Line Half Width	$I_F = 20$ mA	45	35	35	45	nm
Capacitance						
Typ	V = 0	45	45	45	45	pF
Reverse Voltage (V_R)						
Min	$I_R = 100\ \mu A$	5	5	5	5	V
Typ	$I_R = 100\ \mu A$	25	25	25	25	V
Reverse Current (I_R)						
Max	$V_R = 5.0V$	100	100	100	100	μA
Typ	$V_R = 5.0V$	20	20	20	20	nA
Viewing Angle (Total)		28	28	28	28	Degrees

Circle DATA UPDATE No. 1129

National Semiconductor

October 1980



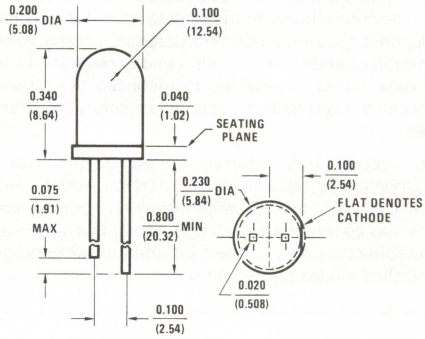
MV5X53, MV5X54 Series LED Lamps

MV5153 Orange Emitter — Diffused Orange Lens
MV5154 Orange Emitter — Lightly Diffused Orange Lens
MV5253 Green Emitter — Diffused Green Lens
MV5254 Green Emitter — Lightly Diffused Green Lens
MV5353 Yellow Emitter — Diffused Yellow Lens
MV5354 Yellow Emitter — Lightly Diffused Yellow Lens
MV5753 Orange-Red Emitter — Diffused Red Lens
MV5754 Orange-Red Emitter — Lightly Diffused Red Lens

Product Description

The MV5X53 and MV5X54 series of LED lamps are LED emitters packaged in colored, diffused lenses. The MV5X53 lens diffusion level produces a soft, wide angle emission pattern. The lighter diffusion level of the MV5X54 lens produces a flood-light (narrow beam) effect.

Physical Dimensions inches (millimeters)



Tolerances ±0.010(±0.254)

Electrical and Optical Characteristics (25°C Free Air Temperature)

Parameter	Conditions	MV5153	MV5154	MV5253	MV5254	MV5353	MV5354	MV5753	MV5754	Units
Forward Voltage (V_F)										
Typ	$I_F = 20$ mA	2.0	2.0	2.2	2.2	2.1	2.1	2.0	2.0	V
Max	$I_F = 20$ mA	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	V
Luminous Intensity (V_L)										
Min	$I_F = 20$ mA	3.0	3.0	0.8	0.9	2.5	3.0	3.0	3.0	mcd
Typ	$I_F = 20$ mA	6.0	8.0	1.5	3.0	6.0	10.0	6.0	8.0	mcd
Peak Wavelength	$I_F = 20$ mA	635	635	565	565	585	585	635	635	nm
Spectral Line Half Width	$I_F = 20$ mA	45	45	35	35	35	35	45	45	nm
Reverse Voltage (V_R)										
Min	$I_R = 100\ \mu A$	5	5	5	5	5	5	5	5	V
Typ	$I_R = 100\ \mu A$	25	25	25	25	25	25	25	25	V
Reverse Current (I_R)										
Max	$V_R = 5.0$V	100	100	100	100	100	100	100	100	μA
Typ	$V_R = 5.0$V	20	20	20	20	20	20	20	20	nA
Viewing Angle (Total)		65	24	65	24	65	24	65	24	Degrees

National Semiconductor

December 1980

PRELIMINARY

NBC82851 256k-Bit Bubble Memory Controller

General Description

The NBC82851 is a dedicated bubble memory controller designed for use with National Semiconductor's NBM2256 256k-bit magnetic bubble memory. The controller is designed so that a minimum of interface circuitry is needed between the controller and the bubble memory devices.

The NBC82851 controller provides all signal timing necessary to drive 1, 2, 4 or 8 bubble memory modules. Start-up and power-down sequencing insures data integrity. The controller performs all data formatting, including redundant loop insertion and deletion, parallel-to-serial conversion, and error detection and correction. An internal data buffer is provided to reconcile the difference between the system bus and bubble memory data transfer rates.

The system bus interface used is the National Semiconductor MICROBUS™ interface, which permits ease of interfacing with a wide variety of microprocessors. Data may be transferred in single or multiple blocks using DMA (Direct Memory Access), interrupt-driven or program-controlled modes of operation.

The NBC82851 is fabricated using National's high performance XMOS technology. It is packaged in a 40-pin DIP and requires a single +5V power supply. The NBC82851 controller is functionally pin compatible with the NBC82853 1-Mbit bubble memory controller.

Features

- Controller for NBM2256 bubble memory
- Complete bubble memory timing generation
- Power fail protection
- MICROBUS™ compatible
- Controls 1, 2, 4 or 8 bubble memories in parallel
- Controls any number of parallel banks of bubble memories
- Error correction capability
- Compatible with 1-Mbit controller
- Standard 40-pin dual-in-line package

Block Diagram

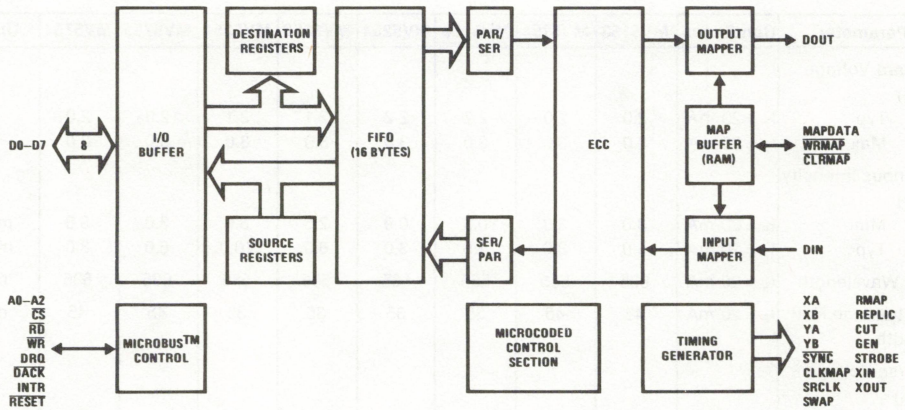


FIGURE 1

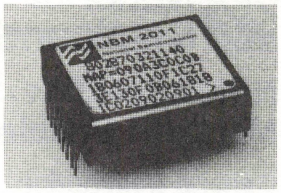
MICROBUS™ is a trademark of National Semiconductor Corp.

Circle DATA UPDATE No. 1131

National Semiconductor

November 1980

NBM2011 1M × 1 Magnetic Bubble Memory Device



General Description

The NBM2011 is a 1,048,576 (2^{20}) bit magnetic bubble memory device. All required magnetic components, including the drive field coils, permanent magnets and protective magnetic shield are integral parts of the device. It is packaged in a 1.3 × 1.1 × 0.36 inch 16-pin DIP.

The NBM2011 features a double-period block-replicate organization with true swap gates on the input track. The storage area is arranged as 512 storage loops of 2048 bit locations each. Additional loops are provided for error correction code and defect tolerance. A map of redundant loop data is provided on-chip in one of two dedicated map loops.

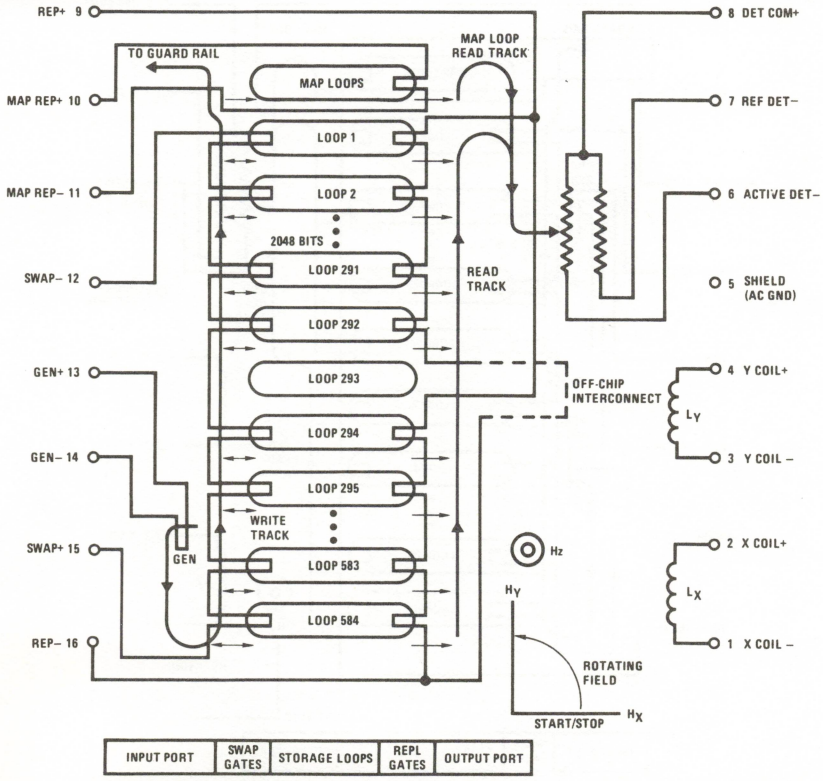
The NBM2011 bubble memory can be operated synchronously or asynchronously. Average access time for a page of data is less than 11.5 ms at 100 kHz. Average power dissipation at 100 kHz is 0.9W. Device performance is guaranteed over a case temperature range of 0°C to 70°C and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements insures excellent conductivity while greatly enhancing resistance to failure from electromigration.

Features

- Solid state
- Non-volatile
- High density
- Low power
- Page-oriented access
- Start/stop capability
- Modular capacity
- On-chip error map
- Single sense channel required
- Swap gate
- Error correction code storage
- 16 pin dual-in-line package

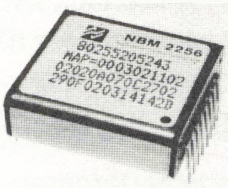
Chip Organization



Circle DATA UPDATE No. 1132

November 1980

National Semiconductor



NBM2256 256k × 1 Magnetic Bubble Memory Device

General Description

The NBM2256 is a 262,144 (2^{18}) bit magnetic bubble memory device. All required magnetic components, including the drive field coils, permanent magnets and protective magnetic shield are integral parts of the device. It is packaged in a 1.3 × 1.1 × 0.36 inch 16-pin DIP.

The NBM2256 features a dual block-replicate organization with true swap gates on the input track. The storage area is arranged as 256 storage loops of 1024 bit locations each. Additional loops are provided for error correction code and defect tolerance. A map of redundant loop data is provided on-chip in one of two dedicated map loops.

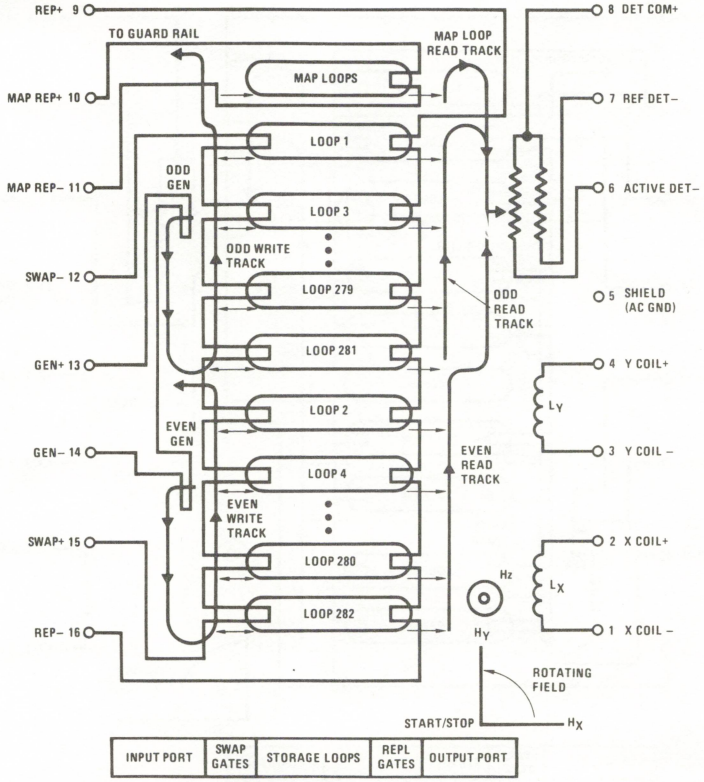
The NBM2256 bubble memory can be operated synchronously or asynchronously. Average access time for a page of data is less than 7 ms at 100 kHz. Average power dissipation at 100 kHz is 0.7W. Device performance is guaranteed over a case temperature range of 0°C to 70°C and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements insures excellent conductivity while greatly enhancing resistance to failure from electromigration.

Features

- Solid state
- Non-volatile
- High density
- Low power
- Page-oriented access
- Start/stop capability
- Modular capacity
- On-chip error map
- Single sense channel required
- Swap gate
- Error correction code storage

Chip Organization



Circle DATA UPDATE No. 1133

National Semiconductor

October 1980

ADVANCE INFORMATION

NMC5295† 16,384-Bit (16,384 × 1) Dynamic RAM

General Description

The NMC5295 is a 16,384 × 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the NMC5295 to be used in page mode operation.

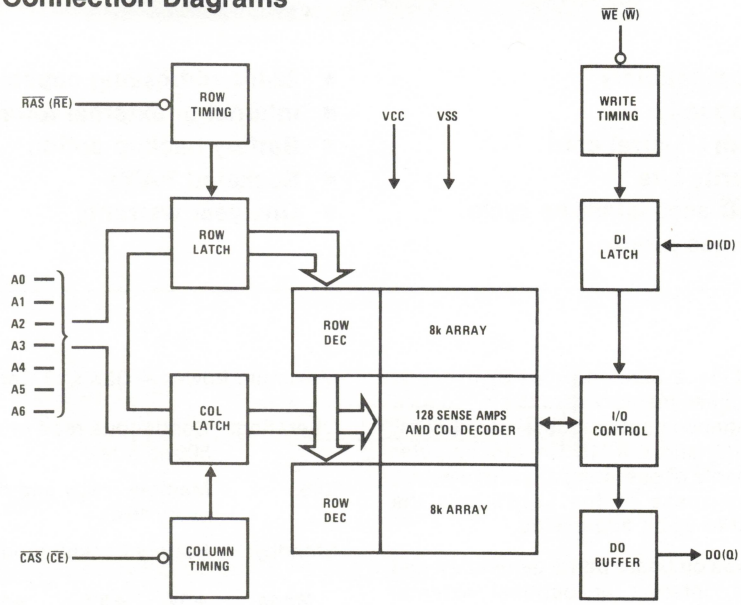
The NMC5295 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including $\overline{RAS}$ ($\overline{RE}$)-only cycle at each of the 128 row addresses.

N-channel triple-polysilicon gate technology, developed by National, is used in the manufacture of the NMC5295. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the NMC5295.

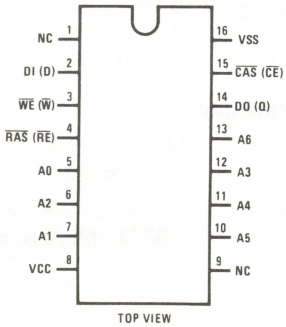
Features

- Single 5V ± 10% supply
- 128 cycle, 2 ms refresh
- Access times: 80 ns, 100 ns, 120 ns
- Low power: 200 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$ ($\overline{CE}$)—non-critical timing
- Read, write, read-modify-write and $\overline{RAS}$ ($\overline{RE}$)-only refresh cycles
- Buried refresh option
- Page mode operation
- Industry standard 16-pin configuration
- TRI-STATE® output
- On-chip substrate bias generator

Block and Connection Diagrams**



Dual-In-Line Package



Pin Names

$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe
$\overline{WE}$ ($\overline{W}$)	Write Enable
A0–A6	Address Inputs
DI (D)	Data Input
DO (Q)	Data Output
VCC	Power (5V)
VSS	Ground

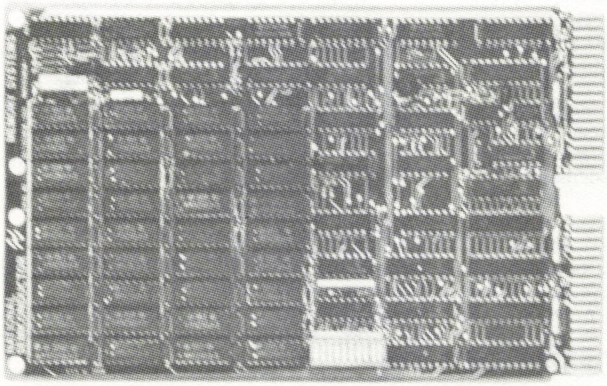
†See the MST™ Program, page 3 of the 1980 Memory Databook.

**Symbols in parentheses are proposed industry standard.

MST™ is a trademark of National Semiconductor Corp.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

NS23L
RAM Memory Card



- **LSI-11/23 compatibility**
- **64K byte capacity**
- **"Dual" width (½-size) card**
- **Optional parity bits**
- **190 ns READ access/490 ns cycle**
- **256 KB address range**
- **22-bit addressing capability**
- **Internal or external refresh**
- **Battery backup option**
- **Socketed RAMs**
- **One year warranty**

Description

National's NS23L is a 32K × 18 (64 KB) dynamic NMOS random access memory card designed as a replacement/ enhancement module for LSI-11, PDP-11/03, LSI-11/2, and LSI-11/23 microcomputer systems. It is capable of operating anywhere within the 128k address space of the LSI-11 plus the ability to respond to 22-bit addressing.

The NS23L features on board parity generation and check capability, internal or optional external refresh functions and battery backup provisions. Optional capacities in 16k increments are available with or without parity (18 or 16 bits).

Performance Specifications

Timing

Function	Mode	Access	Cycle
READ	DATI	190 ns	490 ns
WRITE (byte)	DATO (B)	90 ns	390 ns
R/M/W (byte)	DATIO (B)	700 ns	1000 ns

Maximum Power — 32K × 18 Card

Operating: Continuous read or write cycles at 500 ns rate

Idle: Memory ready and refreshing every 15 us

Standby: Battery backup mode

Mode	+5V	$+5V_{BB}$	+12V	$+12V_{BB}$
Operating	1.5A		0.4A	
Idle	1.5A		0.11A	
Standby		0.775A		0.11A

Compatibility

Memory: MMV11-D and -E or MSV11-D and -E series memories.

Backplanes: Any wired for the LSI-11 "Q" bus, H9270, H9273-A, H9281 or DDV1

National Semiconductor

October 1980

Process 51

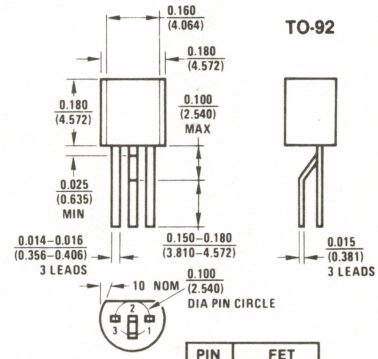
TIS73, TIS74, TIS75 N-Channel JFETs

General Description

The TIS73 thru TIS75 series of N-channel JFETs is designed for analog switch applications requiring low ON resistance and moderate capacitance.

Absolute Maximum Ratings

Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Drain Current	30 mA
Forward Gate Current	50 mA
Total Device Dissipation @ 25°C (Derate above 25°C)	360 mW 2.88 mW/°C
Operating Junction Temperature Range	−65° to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



PIN	FET	
1	D	S*
2	S	D*
3	G	G

*S-D, source and drain pins are interchangeable for most applications.

Electrical Characteristics (25°C unless otherwise noted)

Parameter		Conditions	TIS73 Min	TIS73 Max	TIS74 Min	TIS74 Max	TIS75 Min	TIS75 Max	Units
I_{GSS}	Gate Reverse Current	$V_{GS} = -15V$, $V_{DS} = 0$		−2		−2		−2	nA
		$V_{GS} = -15V$, $V_{DS} = 0$, $T_A = 100°C$		−5		−5		−5	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\ \mu A$, $V_{DS} = 0$	−30		−30		−30		V
$V_{GS(OFF)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V$, $I_D = 4$ nA	−4	−10	−2	−6	−0.8	−4	V
I_{DSS}	Saturation Drain Current	$V_{DS} = 15V$, $V_{GS} = 0$, (Note 1)	50		20	100	8	80	mA
$I_{D(OFF)}$	Drain Cutoff Current	$V_{DS} = 15V$, $V_{GS} = -10V$		−2		−2		−2	nA
		$V_{DS} = 15V$, $V_{GS} = -10V$, $T_A = 100°C$		−5		−5		−5	μA
$r_{ds(ON)}$	Small-Signal Drain-Source On-State Resistance	$V_{GS} = 0$, $I_D = 0$, f = 1 kHz		25		40		60	Ω
$V_{DS(ON)}$	Drain-Source On-State Voltage	$I_D = 20$ mA, $V_{GS} = 0$		0.75					V
		$I_D = 10$ mA, $V_{GS} = 0$				0.5			V
		$I_D = 5$ mA, $V_{GS} = 0$						0.5	V
C_{iss}	Common-Source Short Circuit Input Capacitance	$V_{DS} = 0$, $V_{GS} = -10V$, f = 1 MHz		18		18		18	pF
C_{rss}	Common-Source Short Circuit Reverse Transfer Capacitance	$V_{DS} = 0$, $V_{GS} = -10V$, f = 1 MHz		8		8		8	pF

		TIS73	TIS74	TIS75							
t_d	Turn ON Delay Time	$I_{D(ON)} = 20$ mA	10 mA	5 mA		6		6		10	ns
t_r	Rise Time	$V_{GS(OFF)} = -10V$	−6V	−4V		3		4		10	ns
t_{off}	Turn OFF Delay Time	$V_{DS} = 10V$, $V_{GS(ON)} = 0$, *Figure 1*				25		50		100	ns

Note 1: Pulse test PW 300 μs, duty cycle ≤3%.

Circle DATA UPDATE No. 1136

THE DATA BOOKSHELF: TOOLS FOR THE DESIGN ENGINEER

National Semiconductor's Data Bookshelf is a compendium of information about a product line unmatched in its breadth in the industry. The seventeen independent volumes that comprise the Bookshelf—about 8000 pages—describe in excess of 8100 solid-state devices; devices that span the entire spectrum of semiconductor processes, and that range from the simplest of discrete transistors to microprocessors—those most-sophisticated marvels of modern integrated-circuit technology.

Active and passive devices and circuits; hybrid and monolithic structures; discrete and integrated components... complete electrical and mechanical specifications; charts, graphs, and tables; test circuits and waveforms; design and application information... whatever you need, you'll find it in the designer's ultimate reference source—National Semiconductor's Data Bookshelf.

AUDIO/RADIO HANDBOOK

This 240 page handbook acquaints those involved in audio systems design with National Semiconductor's broad selection of integrated circuits specifically designed for accurate audio reproduction.

Far from just a collection of data sheets, this manual contains detailed discussions, including complete design particulars, covering many areas of audio.

Thorough explanations, complete with real-world design examples make clear several audio areas never before available to the general public.

Page Count: 240 Price: $5.00 Year: 1980

DATA CONVERSION/ACQUISITION DATABOOK

National Semiconductor provides 864 pages of in-depth component and application data about devices in the direct analog signal path before (and after) the digital processor.

With high volume production capabilities, National Semiconductor has become a leader in data conversion/acquisition by utilizing state of the art processes like BI-FET™, linear bipolar, CMOS, thin film, laser trimming, 1^2L, and hybrid.

Selection guides for analog switches/multiplexers, A/D and D/A converters, sample and hold, and voltage reference, and a data conversion/acquisition circuits cross reference guide, along with an alphanumeric index, facilitate quick and easy information selection.

Page Count: 864 Price: $7.00 Year: 1980

THE DISCRETE DATABOOK

480 pages about National Semiconductor's growing line of transistor and FET products are thoroughly cross-referenced and indexed in the Discrete Databook.

Data has been arranged so part numbers can be determined when only process type, industry equivalent, performance requirements, or physical dimensions are known.

Sections include NPN and PNP transistors, the Pro-Electron series, the JEIDA series, and the NA/NB/NR series, plus process characteristics data sheets.

Glossaries of transistor and JFET symbols, and package outlines are in the appendices.

Page Count: 480 Price: $5.00 Year: 1978

48-SERIES MICROCOMPUTER HANDBOOK

This handbook contains detailed design-related information pertaining to the National Semiconductor 48-series single-chip microcomputers and microprocessors.

The material presented is at a level of detail to aid in the design and development of systems using the 48-series microcomputers.

Topics include the 48-series architecture, expansion, and instruction set.

Additional hardware examples, integrated with the required software, and various data sheets of compatible devices are given.

Page Count: 192 Price: $5.00 Year: 1980

BI-FET™ is a trademark of National Semiconductor Corp.

THE IDM2900 MICROPROCESSOR DATABOOK

This 208 page databook covers the full spectrum of the National Semiconductor 2900 family of bipolar microprocessors, comprised of 2900 LSI, memory, and logic components.

The data sheets included consider the architecture, characteristics, and operation of bipolar LSI components.

The IDM2900 product line has added new bit-slices and microsequencers designed with the SCL technique — combining the performance of ECL with low power Schottky I/O compatibility.

National Semiconductor, as ever concerned with optimal system performance, provides useful application notes about bit-slice microprocessor design.

Page Count: 208 Price: $3.00 Year: 1980

THE INTERFACE DATABOOK

In National Semiconductor's Interface Databook, 702 pages of specifications describe one of the industry's broadest lines of interface products.

Over 300 data sheets have been compiled, covering transmission line drivers/receivers, bus transceivers, peripheral/power drivers, level translators/buffers, display drivers, MOS and magnetic memory interface circuits, microprocessor support circuits, applicable TTL and CMOS logic circuits.

An industry cross reference guide gives National Semiconductor's exact replacement for 7 other manufacturers. Product selection guides and a complete product applications section make it easy to find the correct part number for these specialized ICs.

Page Count: 702 Price: $6.00 Year: 1980

LINEAR DATABOOK

The 1980 Linear Databook provides over 1,300 pages of up-to-date information about National's broad line of linear components.

Selection guides, term definitions, features, and diagrams are included for voltage and precision regulators, op amps and instrumentation amplifiers, analog switches/multiplexers, sample and hold, A/D and D/A converters, audio, radio and TV circuits, and transistor/diode arrays.

A usage breakdown is given for components in various industrial, automotive, appliance, functional blocks and telecommunications applications.

Appendices include extended quality and reliability programs, MIL-STD-883/MIL-M-38510 information, and linear and industry cross reference guides.

Page Count: 1376 Price: $9.00 Year: 1980

LINEAR APPLICATIONS HANDBOOK

This 712 page handbook provides a fully indexed and cross referenced collection of 110 linear circuit applications using both monolithic and hybrid circuits from National Semiconductor's broad line of linear products.

Thought provoking applications, written by National's engineers, are an excellent reference source for linear design problems.

Consumer applications; frequency, temperature and drift compensation; and improving signal to noise ratios are just a few of the design requirements considered.

Page Count: 712 Price: $16.00 Year: 1980

MEMORY DATABOOK

National Semiconductor has continued its reputation as a high volume supplier of high quality, cost-effective components by expanding into the design and processing of semiconductor memories.

While developing this state-of-the-art technology, National met the problems of industry standardization by proposing and utilizing new terminology and symbols to make all memory data sheets consistent. Hence, a cohesive, 464 page databook that includes selection guides, diagrams, and test characteristics for RAMs, EPROMs, MOS ROMs, and magnetic bubble memories.

Sections have also been devoted to character generators, memory support circuits, and physical dimensions.

Page Count: 464 Price: $6.00 Year: 1980

MEMORY APPLICATIONS HANDBOOK

More than 200 pages are devoted to in-depth Memory Applications material, including design aids, application notes, technical descriptions and background information for RAMs, ROMs, PROMs and EPROMs. The future of memory technology, and the part that charge coupled and bubble domain memory devices may play, is also thoroughly reviewed. Additionally included are National Semiconductor's reliability report listing and programs, definitions of frequently used acronyms and excerpts from proposed IEEE standards.

Page Count: 256 Price: $11.00 Year: 1979

MOS DATABOOK

The MOS Databook presents 816 pages about COPS™ devices and application information for MOS ROMs, speech synthesis, standard and custom MOS/LSI components.

Fabricated from NMOS, CMOS, and PMOS processes, these devices provide the most cost-effective solution to a system need.

The major emphasis is placed on standard circuits and their use in consumer telecommunications and data processing applications.

Page Count: 816 Price: $6.00 Year: 1980

NSC800 MICROPROCESSOR FAMILY HANDBOOK

Contained in this manual are 224 pages of design-related information about National Semiconductor's 800-family series of high-performance/low-power microprocessor components.

Included are hardware functions, software operations, system support and design considerations for the NSC800 CPU, the NSC810 RAM I/O Timer, and the NSC830 ROM I/O.

Completing this current edition are data sheets, application notes, and physical dimensions for many of the NSC800 components fabricated using the P^2CMOS process.

Page Count: 224 Price: $5.00 Year: 1980

OPTOELECTRONICS HANDBOOK

Discrete LED lamps, multidigit LED numeric arrays and displays, and various custom LED arrays and interface components are catalogued and cross referenced in the 144 page edition of the Optoelectronics Handbook.

Included are absolute ratings, electrical and optical characteristics, recommended array processing, and custom options for this broad line of visible light emitting diodes (LEDs).

Additionally, there is preliminary data for new integrated displays that combine state-of-the-art ICs with the latest in display/readout devices, i.e., bargraph arrays with drivers, 0.3″ and 0.5″ displays with serial drivers.

Page Count: 144 Price: $3.00 Year: 1979

PRESSURE TRANSDUCER HANDBOOK

This is the 144 page handbook of integrated-circuit pressure transducers from National Semiconductor. In addition to complete specifications and a quick selection guide for National's IC transducer products, this edition includes comprehensive information of transducer theory, device structure, reliability and in-depth application data. To improve accuracy in any application, information about circuits designed utilizing the autoreference compensation is thoroughly covered.

Page Count: 144 Price: $3.00 Year: 1977

RELIABILITY HANDBOOK

This 832 page text is addressed not only to reliability specialists, but to designers, specifiers, program managers, and procurement specialists to whom semiconductor reliability is of vital concern.

The first section is a general overview of semiconductor devices, examining tests that include electrical, mechanical, environmental, and visual tests.

Thoroughly explained are the 883B and 883S RETS requirements and their relationship with linear, hybrid, interface, data acquisition, microprocessor and memory, CMOS and bipolar logic high reliability microcircuits made by National Semiconductor.

The handbook is voluminously documented and comprehensively cross referenced.

Page Count: 832 Price: $20.00 Year: 1979

SERIES/80 BOARD LEVEL COMPUTER STARPLEX™ DEVELOPMENT SYSTEM DATABOOK

This databook provides 224 pages of summary information on the complete line of SBC compatible board and system level microcomputer products, as well as information about the National Semiconductor STARPLEX™ development system.

Photos, product overviews, and specifications comprise over 50 BLC and RMC data sheets presented.

The STARPLEX™ Development System section is user-oriented. Featured are the disc operating system, FORTRAN IV and BASIC, the text editor, and options like the IN-SYSTEM EMULATOR™ and STARLINK™. CPU instructions and National Semiconductor training courses conclude the databook.

Page Count: 224 Price: $5.00 Year: 1980

VOLTAGE REGULATOR HANDBOOK

With the variety of fixed and variable regulator technology currently available, the 272 page Voltage Regulator Handbook becomes a must for the selection of three-terminal and dual tracking components that meet the system requirement while utilizing the most cost-effective approach.

Beginning with product selection procedure and a data sheet summary, the text continues with easily accessible information about booster circuitry, power transformer and filter specifications, test methods, manufacturers' cross reference, and extended use applications for National's regulators.

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